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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2894	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/943,512	OSONE ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,15,17-23,25-33,36-50 and 52-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,15,17-23,25-33,36-50 and 52-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 June 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 18, 19, 26, 27, 48, 49 and 54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

> MPEP 2111.01 [R-5] Plain Meaning
>
> I. THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAIN MEANING" UNLESS **>SUCH MEANING IS INCONSISTENT WITH< THE SPECIFICATION
>
> **> Although< claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination [emphasis added].** During examination, the claims must be interpreted as broadly as their terms reasonably allow. In re American Academy of Science Tech Center, 367 F.3d 1359, 1369, 70 USPQ2d 1827, 1834 (Fed. Cir. 2004) (The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation >in light of the specification<.). This means that the words of the claim must be given their plain meaning unless **>the plain meaning is inconsistent with< the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) (discussed below); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004) (Ordinary, simple English words whose meaning is clear and unquestionable, absent any indication that their use in a particular context changes their meaning, are construed to mean exactly what they say. Thus, "heating the resulting batter-coated dough to a temperature in the range of about 400°F to 850°F" required heating the dough, rather than the air inside an oven, to the specified temperature.). **
>
> **>II. IT IS IMPROPER TO IMPORT CLAIM LIMITATIONS FROM THE SPECIFICATION**
>
> **"Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim [emphasis added].** For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." Superguide Corp. v. DirecTV Enterprises, Inc., 358 F.3d 870, 875, 69 USPQ2d 1865, 1868 (Fed. Cir. 2004). See also Liebel-Flarsheim Co. v. Medrad Inc., 358 F.3d 898, 906, 69 USPQ2d 1801, 1807 (Fed. Cir. 2004)(discussing recent cases wherein the court expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be

construed as being limited to that embodiment);< E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003) ("Interpretation of descriptive statements in a patent's written description is a difficult task, as an inherent tension exists as to whether a statement is a clear lexicographic definition or a description of a preferred embodiment. The problem is to interpret claims in view of the specification' without unnecessarily importing limitations from the specification into the claims."); Altiris Inc. v. Symantec Corp., 318 F.3d 1363, 1371, 65 USPQ2d 1865, 1869-70 (Fed. Cir. 2003) (Although the specification discussed only a single embodiment, the court held that it was improper to read a specific order of steps into method claims where, as a matter of logic or grammar, the language of the method claims did not impose a specific order on the performance of the method steps, and the specification did not directly or implicitly require a particular order). See also paragraph *>IV.<, below. **>When< an element is claimed using language falling under the scope of 35 U.S.C. 112, 6th paragraph (often broadly referred to as means or step plus function language)**, the specification must be consulted to determine the structure, material, or acts corresponding to the function recited in the claim. In re Donaldson, 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994) (see MPEP § 2181- § 2186). In In re Zletz, supra, the examiner and the Board had interpreted claims reading "normally solid polypropylene" and "normally solid polypropylene having a crystalline polypropylene content" as being limited to "normally solid linear high homopolymers of propylene which have a crystalline polypropylene content." The court ruled that limitations, not present in the claims, were improperly imported from the specification. See also In re Marosi, 710 F.2d 799, 218 USPQ 289 (Fed. Cir. 1983) ("Claims are not to be read in a vacuum, and limitations therein are to be interpreted in light of the specification in giving them their broadest reasonable interpretation'." 710 F.2d at 802, 218 USPQ at 292 (quoting In re Okuzawa, 537 F.2d 545, 548, 190 USPQ 464, 466 (CCPA 1976)) (emphasis in original). The court looked to the specification to construe "essentially free of alkali metal" as including unavoidable levels of impurities but no more.). Compare In re Weiss, 989 F.2d 1202, 26 USPQ2d 1885 (Fed. Cir. 1993) (unpublished decision - cannot be cited as precedent) (The claim related to an athletic shoe with cleats that "break away at a preselected level of force" and thus prevent injury to the wearer. The examiner rejected the claims over prior art teaching athletic shoes with cleats not intended to break off and rationalized that the cleats would break away given a high enough force. The court reversed the rejection stating that when interpreting a claim term which is ambiguous, such as "a preselected level of force", we must look to the specification for the meaning ascribed to that term by the inventor." The specification had defined "preselected level of force" as that level of force at which the breaking away will prevent injury to the wearer during athletic exertion.**)

*>III. < "PLAIN MEANING" REFERS TO THE ORDINARY AND CUSTOMARY MEANING GIVEN TO THE TERM BY THOSE OF ORDINARY SKILL IN THE ART

"[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." Phillips v. AWH Corp., *>415 F.3d 1303, 1313<, 75 USPQ2d 1321>, 1326< (Fed. Cir. 2005) (en banc). Sunrace Roots Enter. Co. v. SRAM Corp., 336 F.3d 1298, 1302, 67 USPQ2d 1438, 1441 (Fed. Cir. 2003); Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc., 334 F.3d 1294, 1298 67 USPQ2d 1132, 1136 (Fed. Cir. 2003)("In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art."). It is the use of the words in the context of the written description and

customarily by those skilled in the relevant art that accurately reflects both the "ordinary" and the "customary" meaning of the terms in the claims. Ferguson Beauregard /Logic Controls v. Mega Systems, 350 F.3d 1327, 1338, 69 USPQ2d 1001, 1009 (Fed. Cir. 2003) (Dictionary definitions were used to determine the ordinary and customary meaning of the words "normal" and "predetermine" to those skilled in the art. In construing claim terms, the general meanings gleaned from reference sources, such as dictionaries, must always be compared against the use of the terms in context, and the intrinsic record must always be consulted to identify which of the different possible dictionary meanings is most consistent with the use of the words by the inventor.); ACTV, Inc. v. The Walt Disney Company, 346 F.3d 1082, 1092, 68 USPQ2d 1516, 1524 (Fed. Cir. 2003) (Since there was no >express< definition given for the term "URL" in the specification, the term should be given its broadest reasonable interpretation >consistent with the intrinsic record< and take on the ordinary and customary meaning attributed to it by those of ordinary skill in the art; thus, the term "URL" was held to encompass both relative and absolute URLs.); and E-Pass Technologies, Inc. v. 3Com Corporation, 343 F.3d 1364, 1368, 67 USPQ2d 1947, 1949 (Fed. Cir. 2003) (Where no explicit definition for the term "electronic multi-function card" was given in the specification, this term should be given its ordinary meaning and broadest reasonable interpretation; the term should not be limited to the industry standard definition of credit card where there is no suggestion that this definition applies to the electronic multi-function card as claimed, and should not be limited to preferred embodiments in the specification.). The ordinary and customary meaning of a term may be evidenced by a variety of sources, >including "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art."< Phillips v. AWH Corp., *>415 F.3d at 1314<, 75 USPQ2d **>at 1327.< If extrinsic reference sources, such as dictionaries, evidence more than one definition for the term, the intrinsic record must be consulted to identify which of the different possible definitions is most consistent with applicant's use of the terms. Brookhill-Wilk 1, 334 F. 3d at 1300, 67 USPQ2d at 1137; see also Renishaw PLC v. Marposs Societa ' per Azioni, 158 F.3d 1243, 1250, 48 USPQ2d 1117, 1122 (Fed. Cir. 1998) ("Where there are several common meanings for a claim term, the patent disclosure serves to point away from the improper meanings and toward the proper meanings.") and Vitronics Corp. v. Conceptronic Inc., 90 F.3d 1576, 1583, 39 USPQ2d 1573, 1577 (Fed. Cir. 1996) (construing the term "solder reflow temperature" to mean "peak reflow temperature" of solder rather than the "liquidus temperature" of solder in order to remain consistent with the specification.). If more than one extrinsic definition is consistent with the use of the words in the intrinsic record, the claim terms may be construed to encompass all consistent meanings. ** See *>e.g.,< Rexnord Corp. v. Laitram Corp., 274 F.3d 1336, 1342, 60 USPQ2d 1851, 1854 (Fed. Cir. 2001)(explaining the court's analytical process for determining the meaning of disputed claim terms); Toro Co. v. White Consol. Indus., Inc., 199 F.3d 1295, 1299, 53 USPQ2d 1065, 1067 (Fed. Cir. 1999)("[W]ords in patent claims are given their ordinary meaning in the usage of the field of the invention, unless the text of the patent makes clear that a word was used with a special meaning."). Compare MSM Investments Co. v. Carolwood Corp., 259 F.3d 1335, 1339-40, 59 USPQ2d 1856, 1859-60 (Fed. Cir. 2001) (Claims directed to a method of feeding an animal a beneficial amount of methylsulfonylmethane (MSM) to enhance the animal's diet were held anticipated by prior oral administration of MSM to human patients to relieve pain. Although the ordinary meaning of "feeding" is limited to provision of food or nourishment, the broad definition of "food" in the written description warranted finding that the claimed method encompasses the use of MSM for both nutritional and pharmacological purposes.); and Rapoport v. Dement, 254 F.3d 1053, 1059-60, 59 USPQ2d 1215, 1219-20 (Fed. Cir. 2001) (Both intrinsic evidence and the plain meaning of the term "method for treatment of sleep apneas" supported construction of the term as

being limited to treatment of the underlying sleep apnea disorder itself, and not encompassing treatment of anxiety and other secondary symptoms related to sleep apnea.).

The fact that Halliburton can articulate a definition supported by the specification, however, does not end the inquiry. Even if a claim term's definition can be reduced to words, the claim is still indefinite if a person of ordinary skill in the art cannot translate the definition into meaningfully precise claim scope. Having reviewed the remaining two parts of Halliburton's proposed construction, both individually and in combination, in the context of the intrinsic record and the knowledge of a person of ordinary skill in the art, we hold that the ambiguity as to the scope of "fragile gel" cannot be resolved. … *Amgen, Inc. v. Chugai Pharm. Co., Ltd.*, 927 F.2d 1200, 1218 [18 USPQ2d 1016] (Fed. Cir. 1991) (holding that the term "at least about" was indefinite because the patent provided no guidance as to where the line should be drawn between the numerical value of the prior art cited in the prosecution history and the close numerical value in the patent) … However, when a limitation is ambiguous as to the presence or absence of an upper bound, an inquiry into the definiteness of that limitation is warranted. … We note that the patent drafter is in the best position to resolve the ambiguity in the patent claims, and it is highly desirable that patent examiners demand that applicants do so in appropriate circumstances so that the patent can be amended during prosecution rather than attempting to resolve the ambiguity in litigation. … As discussed above, Halliburton's proposed definition of that term is not sufficiently definite because it does not adequately distinguish the fragileness of the invention from disclosed prior art, it is ambiguous as to whether an upper bound of fragileness is contemplated . In other words, Halliburton's proposed construction of "fragile gel" as used in the claims of the '832 patent is indefinite because it is ambiguous as to the requisite degree of the fragileness of the gel, (Halliburton Energy Services Inc. v. M-I LLC, 85 USPQ2d 1654 (Fed. Cir. 2008))

As such, we employ a lower threshold of ambiguity when reviewing a pending claim for indefiniteness than those used by post-issuance reviewing courts. In particular, rather than requiring that the claims are insolubly ambiguous, we hold that if a claim is amenable to two or more plausible claim constructions, the USPTO is justified in requiring the applicant to more precisely define the metes and bounds of the claimed invention by holding the claim unpatentable under 35 U.S.C. §112, second paragraph, as indefinite. The USPTO, as the sole agency vested with the authority to grant exclusionary rights to inventors for patentable inventions, has a duty to guard the public against patents of ambiguous and vague scope. Such patents exact a cost on society due to their ambiguity that is not commensurate with the benefit that the public gains from disclosure of the invention. The USPTO is justified in using a lower threshold showing of ambiguity to support a finding of indefiniteness under 35 U.S.C. §112, second paragraph, because the applicant has an opportunity and a duty to amend the claims during prosecution to more clearly and precisely define the metes and bounds of the claimed invention and to more clearly and precisely put the public on notice of the scope of the patent. As the Federal Circuit recently stated in Halliburton Energy Servs.: When a claim limitation is defined in purely functional terms, the task of determining whether that limitation is sufficiently definite is a difficult one that is highly dependent on context (e.g., the disclosure in the specification and the knowledge of a person of ordinary skill in the relevant art area). We note that the patent drafter is in the best position to resolve the ambiguity in the patent claims, and it is highly desirable that patent examiners demand that applicants do so in appropriate circumstances so that the patent can be amended during prosecution rather than attempting to resolve the ambiguity in litigation. Halliburton Energy Servs. v. M-ILLC 514 F.3d 1244, 1255 [85 USPQ2d 1654] (Fed. Cir. 2008) (emphasis added). Also, the requirement that the applicant clearly and precisely set out the metes and bounds of

> the claimed invention prior to completion of examination of the patentability of the claims furthers the USPTO's duty to issue valid patents. A fundamental principle of patent law is that the claims measure the invention. United Carbon Co. v. Binney & Smith Co., 317 U.S. 228, 232 [55 USPQ 381] (1942). The duty of the PTO is to issue valid claims upon whose language the public can rely. See Keystone Bridge Co. v. Phoenix Iron Co., 95 U.S. 274, 278 (1877) ("[In the Patent Office, applicant's] claim is, or is supposed to be, examined, scrutinized, limited, and made to conform to what he is entitled to."); Burns v. Meyer, 100 U.S. 671, 672 (1880); Graham v. John Deere Co. , 383 U.S. 1, 18 [148 USPQ 459] (1966) ("[T]he primary responsibility for sifting out unpatentable material lies in the Patent Office. To await litigation is—for all practical purposes—to debilitate the patent system."). We realize that our reviewing court has never before set forth a different standard of review for indefiniteness under 35 U.S.C. §112, second paragraph, for pre-issuance pending claims as compared with post-issuance patented claims. The Federal Circuit has, however, noted that a different standard for indefiniteness may be appropriate during prosecution of patent claims. See Exxon Research and Engineering Co. v. U.S., 265 F.3d 1371, 1384 [60 USPQ2d 1272] (Fed. Cir. 2001) ("If this case were before an examiner, the examiner might well be justified in demanding that the applicant more clearly define UL, and thereby remove any degree of ambiguity. However, we are faced with an issued patent that enjoys a presumption of validity.") Accordingly, we adopt this lower threshold standard of ambiguity for indefiniteness for claims during prosecution in keeping with the USPTO's broadest reasonable interpretation standard for claim construction. (Ex parte Miyazaki, 89 USPQ2d 1207 (Bd. Pat. App. & Int. 2008))

There is insufficient antecedent basis for the following claim language:

Re claims 18, 19, 26 and 27: said multilayer wiring substrate.

Re claim 27: that [the thermal conductivity] of the multilayer wiring board.

The scope of the following language is unclear:

Re claim 27: said through holes in the multilayer wiring board having on sides or inside thereof a material of higher thermal conductivity than that of the multilayer wiring board.

Particularly, the multilayer wiring board comprises the material, therefore, it is unclear how the material can have a higher thermal conductivity than the multilayer wiring board.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The undescribed subject matter is the following:

Re claim 27: said through holes in the multilayer wiring board having on sides or inside thereof a material of higher thermal conductivity than that of the multilayer wiring board.

In view of the 112 second paragraph rejection of claim 27, it appears that one skilled in the art would be unable to make and or use the invention because it appears that the multilayer wiring board would have the same thermal conductivity as the material of which it is comprised.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains

subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The undescribed subject matter is the following:

Re claim 27: said through holes in the multilayer wiring board having on sides or inside thereof a material of higher thermal conductivity than that of the multilayer wiring board; than that [the thermal conductivity] of the multilayer wiring board.

To further clarify, there is original disclosure for the material of higher thermal conductivity than particular materials (e.g., "the mother material") of the multilayer wiring board, but not for a thermal conductivity of the multilayer wiring board itself.

In the rejections infra, generally, reference labels and other claim element identifiers are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14, 15, 17-20, 31, 32, 50 and 52 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hayasaka (6809421).

At column 4, lines 12-14; column 7, lines 6-12 and 48-55; column 9, line 61 to column 10, line 7; column 10, lines 60-61; column 12, line 6 to column 13, line 8 to column 14, line 43; and column 28, lines 9-24 and 32-36; Hayasaka discloses the following:

Re claim 14: A multilayer wiring board 1c having "through holes" 13 in a thickness-wise direction, wherein a semiconductor substrate 1b mounted and superimposed on the multilayer wiring board has "through holes" 13 formed in a thicknesswise direction thereof, the through holes of the semiconductor substrate being located directly above the through holes of the multilayer wiring board which form thermal vias 4/15 in the multilayer wiring board:

> A chip for use in a multichip semiconductor device of the present invention has a connect plug that is formed in a through hole that passes through the semiconductor substrate and the interlayer insulating film and adapted to provide an electrical connection for another chip. … The connect plug has also the effect of radiating heat of the chip. … In addition, the metal plugs 4 has the effect of disposing of unwanted heat. … Although the embodiment has been described as comprising three chips, four or more chips can be connected in the same way. Not every chip having the metal plugs 4 need be

> connected with its neighbor by means of the plugs. That is, one or more of the chips may be formed with metal plugs only for the purpose of heat radiation. … As a result, a structure is formed in which the metal film (metal plug)15 has been buried in the hole 13.

and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 15: A multilayer wiring board 1c having "through holes" in a thickness-wise direction which form thermal vias in the multilayer wiring board, wherein a semiconductor substrate 1b mounted and superimposed on the multilayer wiring board has "through holes" formed in a thicknesswise direction thereof, the through holes of the semiconductor substrate being located respectively directly above the through-holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which partly (i.e., in some measure or degree) overlap the through holes of the multilayer wiring board.

Re claim 17: A multilayer wiring board having through holes in a thickness-wise direction which form thermal vias in the multilayer wiring board, wherein a semiconductor substrate mounted on the multilayer wiring board has cross-plane through holes, and heat flows inherently at least one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows

out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 18: The multilayer wiring board according to claim 14 or 15, wherein conductive layers 4/15 are formed on side surfaces of said through holes in said multilayer wiring substrate, or interiors of the through holes in said multilayer wiring substrate comprise a conductive material.

Re claim 19: The multilayer wiring board according to claim 14 or 15, wherein a semiconductor element 1b is mounted, in which conductive layers are formed on side surfaces of said through holes in said multilayer wiring substrate, or interiors of the through holes in said multilayer wiring substrate comprise a conductive material.

Re claim 20: The multilayer wiring board according to claim 14, wherein wirings 19a, 19b, 20a, 20b, which inherently connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate,

and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

Re claim 31: A multilayer wiring board according to claim 15, wherein the through holes in the semiconductor substrate extend between first and second main surfaces of the semiconductor substrate.

Re claim 32: A multilayer wiring board according to claim 14, wherein the through holes in the semiconductor substrate extend between first and second main surfaces of the semiconductor substrate.

Re claim 50: The multilayer wiring board according to claim 14, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 52: The multilayer wiring board according to claim 17, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

MPEP 2112 [R-3] Requirements of Rejection Based on Inherency; Burden of Proof
V. ONCE A REFERENCE TEACHING PRODUCT APPEARING TO BE

SUBSTANTIALLY IDENTICAL IS MADE THE BASIS OF A REJECTION,
AND THE EXAMINER PRESENTS EVIDENCE OR REASONING
TENDING TO SHOW INHERENCY, THE BURDEN SHIFTS TO THE
APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE
"[T]he PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his [or her] claimed product. Whether the rejection is based on inherency' under 35 U.S.C. 102, on prima facie obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same...[footnote omitted]." The burden of proof is similar to that required with respect to product-by-process claims. In re Fitzgerald, 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980) (quoting In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977)).

MPEP 2112.01 [R-3] Composition, Product, and Apparatus Claims
I. PRODUCT AND APPARATUS CLAIMS — WHEN THE STRUCTURE
RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO
THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE
PRESUMED TO BE INHERENT
Where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). "When the PTO shows a sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not." In re Spada, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). Therefore, the prima facie case can be rebutted by evidence showing that the prior art products do not necessarily possess the characteristics of the claimed product.

MPEP 2113 [R-1] Product-by-Process Claims
ONCE A PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS
FOUND AND A 35 U.S.C. 102 /103 REJECTION MADE, THE BURDEN
SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE
"The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. In re Fessmann, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product.

MPEP 2114 [R-1] Apparatus and Article Claims — Functional Language
For a discussion of case law which provides guidance in interpreting the functional portion of means-plus-function limitations see MPEP § 2181 - § 2186.
APPARATUS CLAIMS MUST BE STRUCTUR-ALLY DISTINGUISHABLE
FROM THE PRIOR ART
>While features of an apparatus may be recited either structurally or functionally, claims<directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover

> what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

In addition to the explicit disclosures supra, the structure and composition of the invention of Hayasaka appears to have the following inherent characteristics:

Re claims 14, 15 and 17: inherently thermal vias.

Re claim 17: heat flows inherently at least one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board.

Re claim 20: wirings 19a, 19b, 20a, 20b, which inherently connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

In particular, because the **claimed** structure and composition and the structure and composition of Hayasaka are at least substantially identical, and/or are produced by at least substantially identical processes, a prima facie case of anticipation has been established, and applicant is required to prove that the structure of Hayasaka does not necessarily or inherently possess the characteristics of the instant claimed structure.

Also, the following are statements of intended use:

Re claims 14, 15 and 17: thermal.

Re claim 17: heat flows at least one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board.

Moreover, the statements of intended use do not appear to result in a structural difference between the claimed structure and the structure of applicant's admitted prior art. Further, because the product of applicant's admitted prior art appears to have the same structure as the claimed structure, it appears to be capable of being used for the intended use, and

the statement of intended use does not patentably distinguish the claimed structure from the structure of the admitted prior art. In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963) (Court held that the purpose or intended use of hair curling was of no significance to the structure and process of making). The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)).

Claims 21 and 22 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by applicant's admitted prior art.

Applicant admits as prior art the following:

Re claim 21: A multilayer wiring board having cross-plane through holes 4 in said multilayer wiring board which form "thermal vias" in the multilayer wiring board, wherein said through holes extend in a direction substantially orthogonal to a planar direction of a major surface of the multilayer wiring board, wherein said through holes are distributed in the multilayer wiring board to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board inherently such that a distribution of heat (at least the distribution of heat that is dissipated by the distribution of the through holes in said planar direction) dissipated from the transistor in said planar direction -is substantially identical with a distribution of the through holes in said planar direction.

Re claim 22: A multilayer wiring board having cross-plane through holes in said multilayer wiring board which form thermal vias in the multilayer wiring board, wherein said through holes extend in a direction substantially orthogonal to a planar direction of a major surface of the multilayer wiring board, wherein said through holes are distributed in the multilayer wiring board to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board inherently such that a distribution of heat dissipated from the transistor in said planar

direction is substantially identical with distribution of large and small cross-section areas of the through holes in said planar direction.

For reasons additional to the explicit disclosures supra, the structure and composition of the invention of applicant's admitted prior art appears to have the following inherent characteristics:

Re claim 21: inherently thermal vias; inherently to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with a distribution of the through holes in said planar direction.

Re claim 22: inherently thermal vias; inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with a distribution of large and small cross-section areas of the through holes in said planar direction.

In particular, because the **claimed** structure and composition and the structure and composition of applicant's admitted prior art are at least substantially identical, and/or are produced by at least substantially identical processes, a prima facie case of anticipation has been established, and applicant is required to prove that the structure of the admitted prior art

does not necessarily or inherently possess the characteristics of the instant claimed structure.

In any case, the following are statements of intended use:

Re claims 21 and 22: thermal.

Re claim 21: to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with a distribution of the through holes in said planar direction.

Re claim 22: to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with a distribution of large and small cross-section areas of the through holes in said planar direction.

Moreover, the statements of intended use do not appear to result in a structural difference between the claimed structure and the structure of applicant's admitted prior art. Further, because the product of applicant's admitted prior art appears to have the same structure as the claimed structure, it appears to be capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed structure from the structure of the admitted prior art. In re Otto, 312 F.2d

937, 938, 136 USPQ 458, 459 (CCPA 1963) (Court held that the purpose or intended use of hair curling was of no significance to the structure and process of making). The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)).

In addition, 37 CFR 1.84(p)(4) states:

> The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts.

Therefore, as confirmed by applicant in the specification, at page 21, lines 7-10, identical reference characters, including reference characters 1-

10, of the instant invention and applicant's admitted prior art designate the same part. As such, the same parts designated by identical reference characters would also be capable of being used for the same claimed thermal and heat distribution intended uses.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14, 15, 17-23, 25-33, 36-50 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art and Hayasaka (6809421).

The admitted prior art discloses all of the claim structural limitations except for the relative, overlapping locations of the semiconductor substrate 1 through holes 5 and the wiring board 3 through holes 4 which results in the claimed heat dissipating intended use of the claimed product.

Nonetheless, Hayasaka discloses the claimed relative overlapping locations of the semiconductor substrate 1 through holes 4 and wiring board 3 through holes 5, which, in the obvious combination with the applied prior art, results in the claimed heat dissipating intended use of the claimed product.

Specifically, at page 10, lines 19-24; page 11, lines 12-17; page 12, line 1 to page 16, line 22; page 19, line 24 to page 20, line 8; and page 26, lines 10-17, applicant admits as prior art the following:

Re claim 14: A multilayer wiring board 3 having through holes 4 in a thickness-wise direction, wherein a semiconductor substrate 1 mounted and superimposed on the multilayer wiring board has through holes 5 formed in a thicknesswise direction thereof, the through holes of the semiconductor substrate being located above the through holes of the multilayer wiring board which form thermal vias "thermal via" 4 in the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the multilayer wiring board.

Re claim 15: A multilayer wiring board having through holes in a thickness-wise direction which form thermal vias in the multilayer wiring board, wherein a semiconductor substrate mounted and superimposed on the multilayer wiring board has through holes formed in a thicknesswise direction thereof, the through holes of the semiconductor substrate being located respectively above the through-holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which partly (i.e., in some measure or degree) overlap the multilayer wiring board.

Re claim 17: A multilayer wiring board having through holes in a thickness-wise direction which form thermal vias in the multilayer wiring board, wherein a semiconductor substrate mounted on the multilayer wiring board has cross-plane through holes, and heat flows inherently at least one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the multilayer wiring board.

Re claim 18: The multilayer wiring board according to claim 14 or 15, wherein conductive layers are formed on side surfaces of said through holes in said multilayer wiring substrate, or interiors of the through holes in said multilayer wiring substrate comprise a "conductive" "material".

Re claim 19: The multilayer wiring board according to claim 14 or 15, wherein a semiconductor element is mounted, in which conductive layers "gold plating" are formed on side surfaces of said through holes in said

multilayer wiring substrate, or interiors of the through holes in said multilayer wiring substrate comprise a conductive material.

Re claim 20: The multilayer wiring board according to claim 14, wherein wirings 10, which connect "heating areas" in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

Re claim 21: A multilayer wiring board having cross-plane through holes in said multilayer wiring board which form thermal vias in the multilayer wiring board, wherein said through holes extend in a direction substantially orthogonal to a planar direction of a major surface of the multilayer wiring board, wherein said through holes are distributed in the multilayer wiring board inherently to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction -is substantially identical with a distribution of the through holes in said planar direction.

Re claim 22: A multilayer wiring board having cross-plane through holes in said multilayer wiring board which form thermal vias in the multilayer wiring board, wherein said through holes extend in a direction substantially orthogonal to a planar direction of a major surface of the multilayer wiring board, wherein said through holes are distributed in the multilayer wiring board inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with distribution of large and small cross-section areas of the through holes in said planar direction.

Re claim 23: A multilayer wiring board, wherein a semiconductor substrate having cross-plane through holes, which are connected to emitter wirings 10 connected to "emitters" of heterojunction bipolar transistors "HBTs" and extended through the semiconductor substrate and which have conductive layers "gold plating" on sides thereof or inside thereof, is mounted on the multilayer wiring board, and the cross-plane through holes in the semiconductor substrate and through holes extending through the multilayer wiring board which form thermal vias in the multilayer wiring board are connected to each other, and wherein conductive layers "gold plating" "conductive" "material" are provided on sides of or inside of the connected through holes in the semiconductor substrate and the multilayer

wiring board, and the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the multilayer wiring board.

Re claim 25: A semiconductor device including a plurality of "finger"-shaped emitter electrodes 7 or source electrodes, and at least one via hole 5 which are arranged in rows in a first direction on a semiconductor substrate, wherein the emitter electrodes or the source electrodes are connected to a conductive layer 6 formed on a back surface opposite to a surface, on which the electrodes are formed, through the via hole, and wherein said rows comprising the emitter electrodes or source electrodes, and the via holes are arranged in parallel in a second direction orthogonal to the first direction, and the via holes are positionally shifted from one another ("in a longitudinal direction in the figure [FIG. 11]") in adjacent rows among said rows, or adjacent rows are positionally shifted from one another in the first direction, wherein a multilayer wiring board has through holes which form thermal vias in the multilayer wiring board formed on sides thereof or inside thereof with a conductive layer, and areas, which the via holes of the semiconductor device occupies, overlap areas which the multilayer wiring board occupy in a plane orthogonal to a thickness-wise direction of the multilayer wiring board.

Re claim 26: A multilayer wiring board, wherein emitter electrodes of heterojunction bipolar transistors are arranged on a semiconductor substrate

including through holes, the semiconductor substrate is mounted on a wiring board, which wiring board has cross-plane through holes which form thermal vias in the wiring board, and said through holes in the wiring board have on sides or inside thereof a material of good thermal conductivity, wherein the emitter electrodes are disposed in a group electrically connected by a common emitter wiring 10 located in a plane over the semiconductor substrate, wherein emitter electrodes in a central area of the group are located over areas, and wherein first and second end emitter electrodes are respectively disposed at opposite ends of the emitter electrodes in the central area of the group, the through holes of the semiconductor substrate being located directly above the through holes in said multilayer wiring substrate, and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 27: A multilayer wiring board having through holes which form thermal vias in the multilayer wiring board, wherein emitter electrodes of heterojunction bipolar transistors are arranged in line on a semiconductor substrate, said semiconductor substrate is mounted on said multilayer wiring board, and said multilayer wiring board has cross-plane through holes, said through holes in the multilayer wiring board having on sides or inside thereof a material (the thermal via material) of inherently higher thermal

conductivity than that of the multilayer wiring board, wherein said emitter electrodes are arranged in a line to form "groups", such that all emitter electrodes in a group are connected with a common emitter wiring 10, wherein each group includes central emitter electrodes located between first and second end emitter electrodes, wherein said first and second end emitter electrodes are located, respectively, at opposite ends of the central emitter electrodes, and wherein, with respect to a positional relation viewed from a normal direction to an in-plane surface of said multilayer wiring board, the central emitter electrodes in each of said groups of said emitter electrodes are included in an area.

Re claim 28: A multilayer wiring board according to claim 14, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink 6 located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 29: A multilayer wiring board according to claim 28, wherein the through holes in the semiconductor substrate extend between first and second main surfaces of the semiconductor substrate.

Re claim 30: A multilayer wiring board according to claim 29, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer 2.

Re claim 31: A multilayer wiring board according to claim 15, wherein the through holes in the semiconductor substrate extend between first and second main surfaces of the semiconductor substrate.

Re claim 32: A multilayer wiring board according to claim 14, wherein the through holes in the semiconductor substrate extend between first and second main surfaces of the semiconductor substrate.

Re claim 33: A multilayer wiring board according to claim 32, wherein a plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 36: A multilayer wiring board according to claim 17, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 37: A multilayer wiring board according to claim 36, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 38: A multilayer wiring board according to claim 37, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 39: A multilayer wiring board according to claim 21, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 40: A multilayer wiring board according to claim 39, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 41: A multilayer wiring board according to claim 22, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 42: A multilayer wiring board according to claim 41, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 43: A multilayer wiring board according to claim 23, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 44: A multilayer wiring board according to claim 43, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 45: A multilayer wiring board according to claim 44, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 46: A multilayer wiring board according to claim 25, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 47: A multilayer wiring board according to claim 46, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 48: A multilayer wiring board according to claim 26, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 49: A multilayer wiring board according to claim 48, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 50: The multilayer wiring board according to claim 14, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of the multilayer wiring board.

Re claim 52: The multilayer wiring board according to claim 17, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of the multilayer wiring board.

Re claim 53: The multilayer wiring board according to claim 23, wherein said thicknesswise direction is a direction of a Z-axis of the

multilayer wiring board, and wherein each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of the multilayer wiring board.

Re claim 54: The multilayer wiring board according to claim 26, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of the multilayer wiring board.

In addition to the explicit disclosures supra, the structure and composition of the invention of applicant's admitted prior art appears to have the following inherent characteristics:

Re claims 14, 15, 17, 21-23 and 25-27: inherently thermal vias.

Re claim 17: heat flows inherently at least one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board.

Re claim 21: inherently to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring

board such that a distribution of heat dissipated from the transistor in said planar direction -is substantially identical with a distribution of the through holes in said planar direction.

Re claim 22: inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with distribution of large and small cross-section areas of the through holes in said planar direction.

In particular, because the **claimed** structure and composition and the structure and composition of applicant's admitted prior art are at least substantially identical, and/or are produced by at least substantially identical processes, a prima facie case of anticipation has been established, and applicant is required to prove that the structure of the admitted prior art does not necessarily or inherently possess the characteristics of the instant claimed structure.

Also, the following are statements of intended use:

Re claims 14, 15, 17, 21-23 and 25-27: thermal.

Re claim 17: heat flows at least one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the

semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board.

Re claim 21: to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction -is substantially identical with a distribution of the through holes in said planar direction.

Re claim 22: to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with distribution of large and small cross-section areas of the through holes in said planar direction.

Moreover, the statements of intended use do not appear to result in a structural difference between the claimed structure and the structure of applicant's admitted prior art. Further, because the product of applicant's admitted prior art appears to have the same structure as the claimed structure, it appears to be capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed structure from the structure of the admitted prior art. In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963) (Court held that the purpose or

intended use of hair curling was of no significance to the structure and process of making). The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)).

However, applicant does not appear to explicitly admit as prior art the following:

Re claim 14: the through holes of the semiconductor substrate being located directly above the through holes of the multilayer wiring board, and

having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 15: the through holes of the semiconductor substrate being located respectively directly above the through-holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which partly overlap the through holes of the multilayer wiring board.

Re claim 17: heat flows one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 21: said through holes are distributed in the multilayer wiring board inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a

distribution of heat dissipated from the transistor in said planar direction -is substantially identical with a distribution of the through holes in said planar direction.

Re claim 22: said through holes are distributed in the multilayer wiring board inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with distribution of large and small cross-section areas of the through holes in said planar direction.

Re claim 23: the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes in the multilayer wiring board.

Re claim 25: areas, which the via holes of the semiconductor device occupies, overlap areas which the through holes of the multilayer wiring board occupy in a plane orthogonal to a thickness-wise direction of the multilayer wiring board.

Re claim 26: the emitter electrodes in the central area of the group are located over areas which the through holes in the wiring board occupy, and wherein the first and second end emitter electrodes protrude from the areas which the through holes in the wiring board occupy.

Re claim 27: the central emitter electrodes in each of said groups of said emitter electrodes are included in an area which said through holes in said multilayer wiring substrate occupy, but the first and second end emitter electrodes of each of said groups of said emitter electrodes protrude from the area which said through holes in said multilayer wiring substrate occupy.

Re claim 50: an entirety of each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 54: an entirety of each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 52: an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 53: an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Nevertheless, as cited supra, Hayasaka discloses following:

Re claim 14: the through holes 13 of the semiconductor substrate 1b being located directly above the through holes 13 of the multilayer wiring board 1c, and having areas projected onto the multilayer wiring board,

perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 15: the through holes of the semiconductor substrate being located respectively directly above the through-holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which partly (i.e., in some measure or degree) overlap the through holes of the multilayer wiring board.

Re claim 17: heat flows at least one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 21: said through holes are distributed in the multilayer wiring board to be aligned relative to at least one through hole of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of

heat dissipated from the semiconductor substrate in said planar direction -is substantially identical with a distribution of the through holes in said planar direction.

Re claim 22: said through holes are distributed in the multilayer wiring board to be aligned relative to at least one through hole of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the semiconductor substrate in said planar direction is substantially identical with distribution of large and small cross-section areas of the through holes in said planar direction.

Re claim 23: the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes in the multilayer wiring board.

Re claim 25: areas, which the via holes of the semiconductor device occupies, overlap areas which the through holes of the multilayer wiring board occupy in a plane orthogonal to a thickness-wise direction of the multilayer wiring board.

Re claim 50: an entirety of each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 54: an entirety of each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 52: an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 53: an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Moreover, it would have been obvious to combine this disclosure of Hayasaka with the disclosure of applicant's admitted prior art because it would facilitate heat dissipation from the product of the admitted prior art.

Also, in the above combination of applicant's admitted prior art and Hayasaka, the following claimed structure would inherently result:

Re claim 26: the emitter electrodes in the central area of the group are located over areas which the through holes in the wiring board occupy, and wherein the first and second end emitter electrodes protrude from the areas which the through holes in the wiring board occupy.

Re claim 27: the central emitter electrodes in each of said groups of said emitter electrodes are included in an area which said through holes in said multilayer wiring substrate occupy, but the first and second end emitter

electrodes of each of said groups of said emitter electrodes protrude from the area which said through holes in said multilayer wiring substrate occupy.

To further clarify, when the central emitter electrodes 7 in each of said groups of emitter electrodes illustrated in the prior art FIG. 4 are combined with Hayasaka to be included in an area which said through holes occupy as illustrated in FIG. 2c, the first and second end emitter electrodes (illustrated in FIGS. 2c and 4, not individually labeled) of each of said groups of said emitter electrodes protrude from the area which the through holes occupy.

Applicant's remarks filed on 08-12-09, 01-04-10, 03-09-10 and 06-08-10 have been fully considered, treated or rendered moot by the restatement of the Office action supra, addressed infra and/or adequately addressed previously of record.

Applicant argues:

> Concerning heat dissipation, the only disclosure provided in Hayasaka is an illustration of a radiation fin 39 placed on a top surface of the uppermost chip in the stacked chip shown in Fig. 18. This has absolutely nothing to do with the claimed thermal via arrangements, and the relative locations of elements with regard to the thermal vias, defined in the present amended claims.

This argument is respectfully traversed because, as elucidated in the rejection, the alleged illustration of a radiation fin 39 is not the only disclosure of Hayasaka of the claimed heat dissipation limitations.

Moreover, Hayasaka is not necessarily applied to the rejection for this disclosure.

Also, applicant contends:

> In the Office Action, it is argued that the position of the plugs 4 for a chip 1b shown in Fig. 5 of Hayasaka overlaps with a solder bump 8 formed in the chip 1c in a thicknesswise direction. However, the through plug 4 and the solder bump 8 in Hayasaka are bonded to one another, thereby simply forming a wiring between them.

These contentions are respectfully traversed because there is no such Office argument that the position of the plugs 4 for chip 1b in shown in Fig. 5 of Hayasaka overlaps with a solder bump 8 formed in the chip 1c in a thicknesswise direction.

Applicant further asserts:

> Although it is also argued in the Office Action that combining the structure of Hayasaka with the admitted prior art shown in Fig. 3 of the present application would render the present claims obvious, it is respectfully submitted since there is no discussion whatsoever concerning the use of the through holes 4 or the solder bumps 8 in Hayasaka for heat dissipation purposes, there is absolutely no motivation for the claimed combination.

These assertions are respectfully traversed because any alleged lack of discussion whatsover concerning the use of the through holes 4 or the solder bumps 8 in Hayasaka for heat dissipation purposes would not preclude motivation for the claimed combination.

In any case teaching, suggestion or motivation to combine the applied prior art is unnecessary:

> The obviousness inquiry cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007))

> The applicant and the examiner have apparently assumed that there always must be 'motivation' to combine teachings of the prior art to support a rejection based on §103(a). The assumption is not correct. The word 'motivation' or a word similar to 'motivation' does not appear in 35 U.S.C. § 103(a). While a finding of 'motivation' supported by substantial evidence probably will support combining teachings of different prior art references to establish a *prima facie* obviousness case, it is not always necessary. For example, where a claimed apparatus requiring Phillips head screws differs from a prior art apparatus describing the use of flathead screws, it might be hard to find motivation to substitute flathead screws with Phillips head screws to arrive at the claimed invention. However, the prior art would make it more than clear that Phillips head screws and flathead screws are viable alternatives serving the same purpose. Hence, the prior art would 'suggest' substitution of flathead screws for Phillips head screws albeit the prior art might not 'motivate' use of Phillips head screws in place of flathead screws. What must be established to sustain an obviousness rejection is a legally sufficient rationale as to why the claimed subject matter, as a whole, would have been obvious notwithstanding a difference between claimed subject matter and a reference which is prior art under 35 U.S.C. § 102. Once a difference is found to exist, then the examiner must articulate a legally sufficient rationale in support of a §103(a) rejection. (Ex parte Jones, 62 USPQ2d 1206 (BdPatApp&Int 2001)

To this end, the instant Office provides legally sufficient rationale as to why the claimed subject matter, as a whole, would have been obvious.

In addition, applicant alleges:

> If heat is conducted between the through holes 4 and the solder bumps 8 in Hayasaka, the heat from the semiconductor substrate will be diffused in an in-plane direction and will then be conducted in the through plug and the solder bump in a cross-plane direction of the substrate. This would result in generated heat having to effectively be bent from the in-plane direction to the cross-plane direction, which is completely different than the arrangements provided in the present claims for conducting heat in a substrate in a cross-plane direction.

These allegations are respectfully traversed because Hayasaka is not necessarily applied for a disclosure of heat is conducted between the through holes 4 and the solder bumps 8.

Also, the allegations are respectfully deemed unpersuasive because they are unsupported by proof or a showing of facts; hence, they essentially amount to mere conjecture and are of no probative value. See MPEP 716.01(c), and, Ex parte Gray, 10 USPQ2d 1922 (Bd. Pat. App. & Inter. 1989) (statement in publication dismissing the "preliminary identification of a human b - NGF - like molecule" in the prior art, even if considered to be an expert opinion, was inadequate to overcome the rejection based on that prior art because there was no factual evidence supporting the statement); In re Beattie, 974 F.2d 1309, 24 USPQ2d 1040 (Fed. Cir. 1992) (declarations of seven persons skilled in the art offering opinion evidence praising the merits of the claimed invention were found to have little value because of a lack of factual support); Ex parte George, 21 USPQ2d 1058 (Bd. Pat. App. & Inter. 1991) (conclusory statements that results were "unexpected," unsupported by objective factual evidence, were considered but were not found to be of substantial evidentiary value).

Applicant also argues:

> In any event, it is respectfully submitted that it represents complete hindsight, solely with benefit of the applicants invention, to propose modification of the admitted prior art using Hayasaka, which fails to provide any discussion concerning heat dissipation using its plugs 4 and the solder bumps 8.

This argument is respectfully traversed because Hayasaka is not necessarily applied to the rejection for a disclosure concerning heat dissipation using its plugs 4 and the solder bumps 8.

In any case, it has been recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning; yet, so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was conceived, and so long as it does not include knowledge gleaned only from applicant's disclosure, such a reconstruction is proper. In re McLaughlin, 443 F.2d 1392; 170 USPQ 209 (CCPA 1971). To this end, it is respectfully submitted that these criteria are satisfied in the rejection of the instant claims.

In addition, applicant asserts:

> Hayasaka simply shows a stacking arrangement for electrical connections, and, as such, would not be something one would ordinarily consider when looking at the admitted prior art of the present application.

These assertions are respectfully traversed because, as elucidated in the Office action, Hayasaka discloses more than simply a stacking arrangement for electrical connections.

Insofar as this is an argument that Hayasaka is nonanalogous art, it is noted that arguments that the alleged anticipatory prior art is nonanalogous art or teaches away from the invention or is not recognized as solving the

problem solved by the claimed invention, are not germane to a rejection under section 102. See MPEP 2131.05.

In any case, Hayasaka is clearly analogous art, because, as elucidated in the rejection, one of ordinary skill in the art could implement a predictable variation of Hayasaka, and would see the benefit of doing so, in order to arrive at the claimed invention. Indeed:

> When a work is available in one field, design incentives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, §103 likely bars its patentability. Moreover, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill. (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007))

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

/David E Graybill/
Primary Examiner, Art Unit 2894